Au8310 High Efficiency Low Quiescent Current Buck-Boost Converter with I2C Interface

General Description

The Au8310 is a high-current, buck-boost switching converter for systems using new battery chemistries. It maintains voltage regulation while providing excellent efficiency and very low output voltage ripple when the input voltage is close to the output voltage.

The Au8310 is capable of delivering at least 2.5A continuous output current (VOUT=3.3V) across a battery voltage range of 2.5V to 4.5V. This maximizes the energy utilization of advanced, single-cell Li-ion battery chemistries that have significant capacity left at voltages below the system voltage.

The Au8310 supports a broader set of programmable features that can be accessed using an I2C interface. With a programmable output voltage range of 1.8V to 5.2V, the Au8310 is ideal for applications which require dynamically changing supply voltages. A programmable slew rate can be selected to provide smooth transitions between different output voltage settings.

The Au8310 is available in a 15 bump, 0.4mm pitch WLCSP (1.38mmx 2.28mm) with a 2.5MHz switching frequency, which further reduces the size of external components.

Features

- Automatic and Seamless Transition Between Buck, Buck-Boost and Boost operation.
- Maintains Steady Output Voltage at Wide Input Voltage Range from 2.3V to 5.5V.
- Output Current:
  - 2.5A for V_{IN}≥2.5V, V_{OUT}=3.3V;
  - 2.5A for V_{IN}≥2.8V, V_{OUT}=3.5V.
  - 3A 2%duty pulse current(T=60s) for V_{IN}=3.6V, V_{OUT}=4.7V.
- 2.5MHz Typical Switching Frequency.
- Integrated Soft Start.
- I2C interface (Up to 1MHz).
- Programmable Output Voltage and Slew-rate with I2C interface.
- VSEL Pin to toggle between two output voltage presets.
- High Efficiency: Up to 95.5%.
- 15μA V_{IN} Quiescent Current when ENABLE BIT=0 in CONTROL Register.
- EN pin Shutdown Function with Less Than 1μA Quiescent Current.
- Output Capacitor Discharge Function to Bleed Output.
- Over-Temperature Protection, Over-Current Protection, Short Circuit Protection and Input Voltage Protection, Over Output Voltage Protection.
- Small 1.38mmx2.28mm, 15-pin WLCSP.

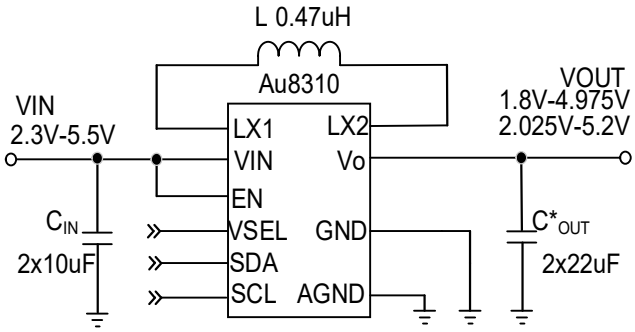


Figure 1 Simplified Schematic

* When VIN<=2.5V, 3x22uF capacitors are recommended for C_{OUT}.

Application

- System Pre-Regulator (Smartphone, Tablet, EFT Terminal, Telematics)
- Point-of-Load Regulation (Wired Sensor, Port/Cable Adapter and Dongle)
- Fingerprint, Face-ID, Camera Sensors (Smartphone, Electronic Smart Lock, IP Network Camera)
- RF Amplifier Supply (Smart Sensors)
- Thermoelectric Device (TEC/TEM) Supply (Datacom, Optical Modules, Cooling/Heating)

Table of Contents

1 Pin Configuration and Functions

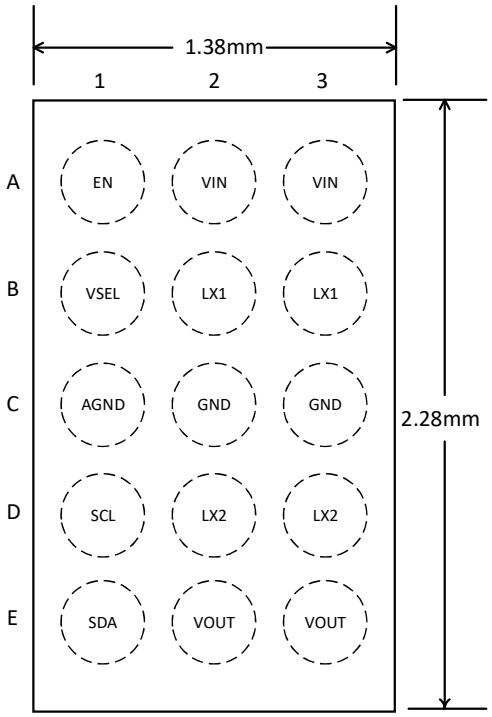


Figure 2 15-Pin WLCSP Package Top View

Table 1 Pin Functions

Pin number	PIN Name	I/O	Description
A1	EN	I	Enable pin. Set high to enable the device and set low to disable the device. It must not be left floating.
B1	VSEL	I	This pin selects which VOUT register is active. When a low logic level is applied to this pin, the VOUT1 register sets the output voltage. When a high logic level is applied to this pin, the VOUT2 register sets the output voltage. This pin must not be left floating.
C2, C3	GND	-	Power Ground.
B2, B3	LX1	-	The Switching node pin of the buck side.
D2, D3	LX2	-	The Switching node pin of the boost side.
A2, A3	VIN	-	Power supply for the power stage.
E2, E3	VOUT	-	Buck-boost converter output.
C1	AGND	-	Analog Ground.
D1	SCL	I/O	I2C serial interface clock. Pull this pin up to the I2C bus voltage with a resistor or a current source.
E1	SDA	I/O	I2C serial interface data. Pull this pin up to the I2C bus voltage with a resistor or a current source.

2 Specifications

Table 2 Absolute Maximum Ratings

Over operation junction temperature range (unless otherwise noted) (1)

Symbol	Parameter	Min	Typ.	Max	Units
V_I	Input Voltage (VIN, LX1, LX2, VOUT, EN, VSEL, SDA, SCL) (2)	-0.3		6	V
T_{OPR}	Operating junction temperature	-40		150	°C
T_{STG}	Storage temperature	-65		150	°C

Notes:

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Expose to absolute maximum rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal, unless otherwise noted.

Table 3 Recommended Operation conditions

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Units
V_{IN}	Input Voltage	2.3		5.5	V
V_{OUT}	Output Voltage (High range)	2.025		5.200	V
	Output Voltage (Low range)	1.800		4.975	
SCL, SDA, VSEL	High-level input voltage	1.3		V_{IN}	V
SCL, SDA, VSEL	Low-level input voltage	0		0.3	V
EN	EN input voltage	0		V_{IN}	V
V_{OUT}=3.3V,V_{IN}≥2.5V	Output current (1)			2.75	A
V_{OUT}=3.5V,V_{IN}≥2.5V				2.6	
V_{OUT}=3.5V,V_{IN}≥2.8V				3.3	
V_{OUT}=3.3V,V_{IN}≥3V				4.4	
C_{IN} (2)	Input capacitance	8			μF
C_O (2)	Output capacitance	13	16		μF
L	Inductance	0.39	0.47	0.56	μH
T_J	Operating junction temperature range	-40		125	°C
T_A	Operating free-air junction temperature range	-40		85	°C

Notes:

(1) The device can sustain the maximum recommended output current only for short durations before its junction temperature gets too hot. Users must verify that the thermal performance of the end application can support the maximum output current.

(2) Effective capacitance after DC bias effects have been considered.

Table 4 ESD Ratings

Symbol	Parameter	Condition	Value	Units
$V_{(ESD)}$	Electrostatic Discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22- C101(2)	±500	V

Notes:

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process

Table 5 Thermal Characteristics

Symbol	Thermal Metric	Value	Units
$R_{\theta JA}$	Junction-to-ambient thermal resistance	75.2	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	16.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.1	°C/W

Notes:

Power rating at a specific ambient temperature TA should be determined with a junction temperature of 125 °C. Thermal management of PCB should strive to keep the junction temperature at or below 125 °C for best performance and long-term reliability.

Table 6 Electrical Characteristics

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted). Typical values are at VIN=3.6V, VOUT=3.3V and TJ = 25°C (unless otherwise noted).

Symbol	Parameter	Condition	Min	Typ	Max	Units
Power Supply						
V_{IN}	Supply Voltage (VIN Pin)	V_{IN}	2.3		5.5	V
$V_{IN(UVLO)}$	V_{IN} internal UVLO threshold and hysteresis	V_{IN} rising	2.1	2.2	2.3	V
$V_{IN(HYS)}$		UVLO threshold voltage hysteresis		150		mV
I_{SD}	V_{IN} shutdown supply current	EN=0V, V_{IN}=3.6V, Vo=0V,TJ=25℃		0.35		μA
I_Q	V_{IN} operating current	EN=3.6V, VIN=3.6V, Io=0A (none switching), Vo=3.3V, TJ=25℃		33		μA
I_Q		EN=3.6V, VIN=3.6V, Output disabled by ENABLE bit in Control Register, Vo=0V, TJ=25℃		15		μA
Logic Signals						
$V_{IH(EN)}$	Enable threshold	Rising	1.07	1.10	1.13	V
$V_{IL(EN)}$		Falling	0.97	1.00	1.03	V
$V_{EN(HYS)}$		EN Hysteresis voltage	40	100		mV
V_{IH}	VSEL/SCL/S DA threshold	Rising			1.2	V
V_{IL}		Falling	0.4			V
I_{IH}	High-level input current	VSEL=SDA=SCL=1.8V, no pullup resistor		±0.01	±0.1	μA
I_{IL}	Low-level input current	VSEL=SDA=SCL=0V, no pullup resistor		±0.01	±0.1	μA
I_{SL}	Low-level sink current	SDA=0.4 V	20			mA
I_{IB}	EN pin Input bias current	EN=0V to 5.5V		±0.01	±0.1	μA
MOSFET						
$R_{DS\_HS\_Buck}$	High- side switch resistance [1]	VIN=3V, VOUT=3.3 V, Io=200mA		38		mΩ
$R_{DS\_LS\_Buck}$	Low- side switch resistance [1]	VIN=3V, VOUT=3.3V, Io=200mA		15		mΩ
$R_{DS\_HS\_Boost}$	High- side switch resistance [1]	VIN=3V, VOUT=3.3V, Io=200mA		45		mΩ
$R_{DS\_LS\_Boost}$	Low- side switch resistance [1]	VIN=3V, VOUT=3.3V, Io=200mA		12		mΩ
Output Voltage Regulation						
	VOUT Range	High Range	2.025		5.200	V
		Low Range	1.800		4.975	V
	VOUT Accuracy	PWM Mode	-1.5		1.5	%
		PFM Mode	-1.5		3.5	%
V_{OUT}	VOUT default output voltage (RANGE=0)	VSEL=Low		3.30		V
		VSEL=High		3.45		
$\Delta V_{OUT} / \Delta I_{OUT}$	Load Regulation (PWM)	VIN =3.6V, VOUT=3.3V, Io step from 0.2A to 2A		5		μV/mA
$\Delta V_{OUT} / \Delta I_{OUT}$	Load Regulation (PFM)	VIN=3.6V, VOUT=3.3V, Io step from 0A to 0.2A		400		μV/mA
$\Delta V_{OUT} / \Delta V_{IN}$	Line Regulation (PWM)	VOUT=3.3V, Io=1A, VIN sweep from 2.5V		5		mV/V

Symbol	Parameter	Condition	Min	Typ	Max	Units
		to 5.5V				
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation (PFM)	VOUT=3.3V, Io=0.2A, VIN sweep from 2.5V to 5.5V		12.5		mV/V

[1] Measured at Pins.

Table 7 Electrical Characteristics (Continued)

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted). Typical values are at VIN=3.6V, VOUT=3.3V and T_J = 25°C (unless otherwise noted).

Symbol	Parameter	Condition	Min	Typ	Max	Units
Current Limit						
I_{LIM_Boost}	High- side switch current limit threshold	VIN=2.9V, VOUT=3.6V, T_J = 25°C	5.2	5.85	6.5	A
I_{LIM_Buck}		VIN=5V, VOUT=3.3V, T_J = 25°C	3.8	4.5	5.2	A
Power Good						
$V_{R(PG)}$	Power-good threshold	Rising threshold		95%V_{OUT}		V
$V_{F(PG)}$		Falling threshold		90%V_{OUT}		
$t_{d(PG)}$	Power-good delay	VOUT falling		50		μs
Input Over-voltage Protection						
$V_{IVP(VTH)}$	VIN OVP rising threshold	VIN increases		5.7		V
$V_{IVP(HYS)}$	VIN OVP hysteresis	VIN decreases		100		mV
Thermal Shutdown						
T_{SD}	Thermal shutdown	Shutdown, temperature increasing		150		°C
	Thermal shutdown hysteresis	Restart, temperature decreasing		20		°C
Switching Frequency						
f_{sw}	Switching Frequency	CCM Mode	2.1	2.5	2.9	MHz
I2C Interface						
Address	Device I2C Address	7-bit slave address		0x75		
Soft-Start and Soft Discharge						
$t_{d(EN)}$	Soft-start and Soft-discharge	Delay between a rising edge on the EN pin and the start of the output voltage ramp.T_J=25°C, VIN=3.6V		320		μs
$V_{OUT\_RiseTime}$		Time from when VOUT starts rising to VOUT reaches 95% target voltage. Buck mode. VIN=3.6V, VOUT=3.3V, Io=100mA.		370		μs
I_{VOUT_DIS}		VOUT discharge current, VIN=3.6V, VOUT≥0.8V	50			mA
PFM/PWM Transient						
	Load Current Threshold PFM to PWM	VIN=3.6V, VOUT=3.3V		850		mA
	Load Current Threshold PWM to PFM	VIN=3.6V, VOUT=3.3V		250		
Output Over-voltage Protection						
$V_{OUT\_OVP\_R}$	VOUT Over Voltage Protection Threshold	VIN=3.6V, VOUT=3.3V, VOUT OVP Rising Threshold		5.82		V
$V_{OUT\_OVP\_F}$		VIN=3.6V, VOUT=3.3V, VOUT OVP Falling Threshold		5.65		V

Table 8 Timing Requirements

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{SCL}	SCL clock frequency	Stand mode	0		100	kHz
		Fast Mode	0		400	
		Fast mode plus	0		1000	
t_{LOW}	Low period of the SCL clock	Stand mode	4.7			µs
		Fast Mode	1.3			
		Fast mode plus	0.5			
t_{HIGH}	High period of the SCL clock	Stand mode	4.0			µs
		Fast Mode	0.6			
		Fast mode plus	0.26			
t_{BUF}	Bus free time between a STOP and a START condition	Stand mode	4.7			µs
		Fast Mode	1.3			
		Fast mode plus	0.5			
$t_{SU;STA}$	Set-up time for a repeated START condition	Stand mode	4.7			µs
		Fast Mode	0.6			
		Fast mode plus	0.26			
$t_{HD;STA}$	Hold time (repeated) START condition	Stand mode	4.0			µs
		Fast Mode	0.6			
		Fast mode plus	0.24			
$t_{SU;DAT}$	Data set-up time	Stand mode	250			ns
		Fast Mode	100			
		Fast mode plus	50			
$t_{HD;DAT}$	Data hold time	Stand mode	0			µs
		Fast Mode	0			
		Fast mode plus	0			
t_r	Rise time of both SDA and SCL signals	Stand mode			1000	ns
		Fast Mode	20		300	
		Fast mode plus			120	
t_f	Fall time of both SDA and SCL signals	Stand mode			300	ns
		Fast Mode	$20 \times V_{DD}/5.5$		300	
		Fast mode plus	$20 \times V_{DD}/5.5$		120	
$t_{SU;STO}$	Set-up time for STOP condition	Stand mode	4			µs
		Fast Mode	0.6			
		Fast mode plus	0.26			
$t_{VD;DAT}$	Data valid time	Stand mode			3.45	µs
		Fast Mode			0.9	
		Fast mode plus			0.45	
$t_{VD;ACK}$	Data valid acknowledge time	Stand mode			3.45	µs
		Fast Mode			0.9	
		Fast mode plus			0.45	
C_b	Capacitive load for each bus line	Stand mode			400	pF
		Fast Mode			400	
		Fast mode plus			550	

Table 9 Switching Characteristics

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted). Typical values are at VIN=3.6V, VOUT=3.3V and TJ = 25°C (unless otherwise noted).

Symbol	Parameter	Condition	Min	Tpy	Max	Units
SR	Slew rate of internal ramp during dynamic voltage scaling	SLEW=00b, Ramp-PWM operation		±1		V/ms
		SLEW=01b, Ramp-PWM operation		±2.5		
		SLEW=10b, Ramp-PWM operation		±5		
		SLEW=11b, Ramp-PWM operation		±10		
$t_{d(VSEL)}$	Delay between rising edge of VSEL and start of DVS ramp	Measured from rising edge of VSEL to start of ramp.			5	μs
$t_{w(VSEL)}$	VSEL pulse duration	VSEL = high or low	5			μs

3 Typical Performance Curves

Table10 lists the components that were used for the measurement waveforms contained in the following pages.

Table 10 Switching Characteristics

Reference	Description	Part Number	Manufacture
C_{IN}	Capacitor, 2x10μF,10V, 0603, Ceramic	GRM188R61A106ME69	Murata
C_{OUT}	Capacitor, 2x22μF, 10V, 0603, Ceramic	GRM187R61A226ME15	Murata
L1	Inductor, 0.47μH	XFL4015-471MEC	Coil craft
U1	Integrated circuit	Au8310	Ningbo Aura Semiconductor Co., Ltd.

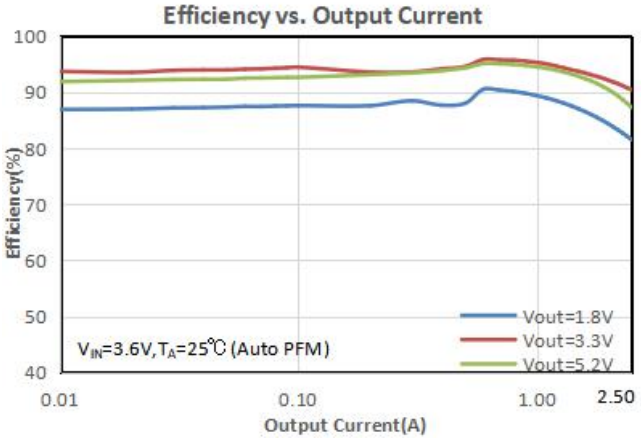


Figure 3 Efficiency versus Output Current (ultra-sonic enable)

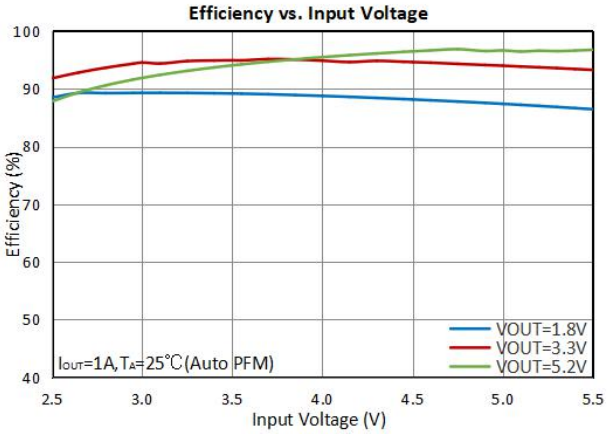


Figure 4 Efficiency versus Input Voltage (ultra-sonic enable)

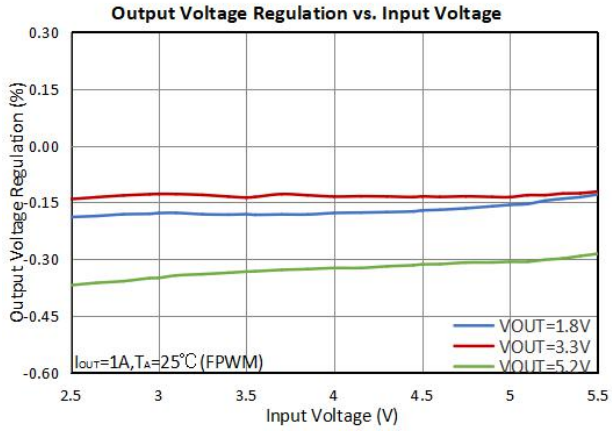


Figure 5. Line Regulation

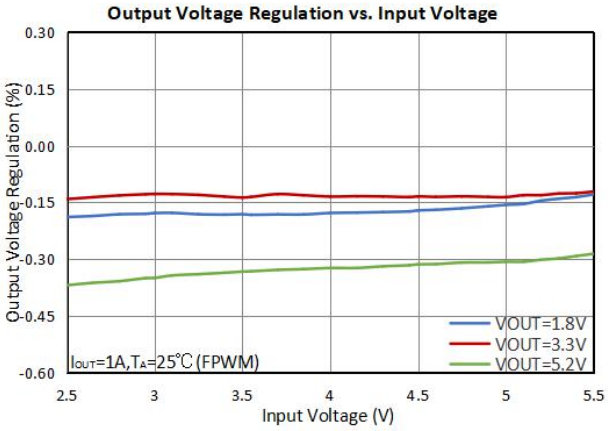
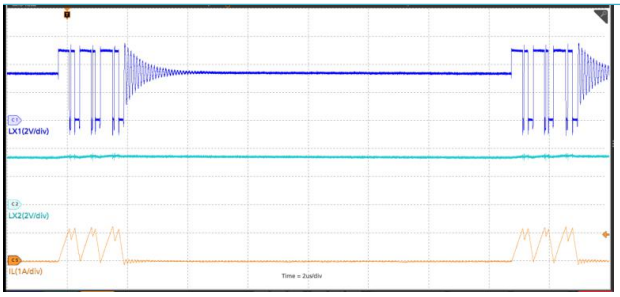
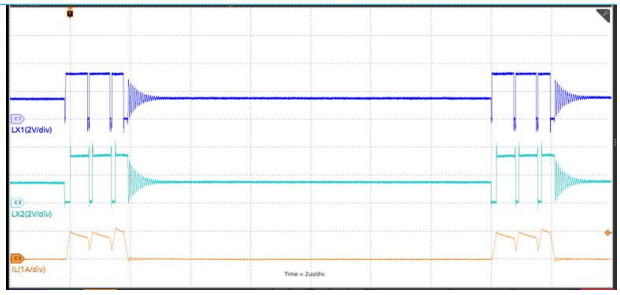


Figure 6. Load Regulation



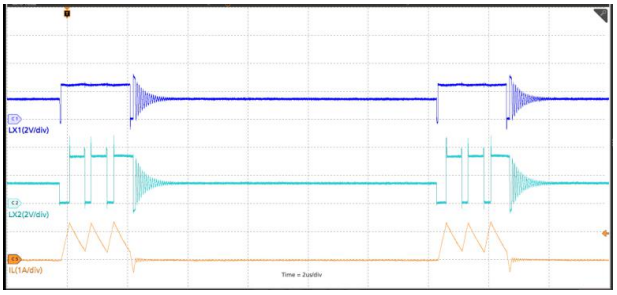
VIN=5V, PFM, T_A=25°C, V_O=3.3V, I_O=100mA

Figure 7 PFM Switching Waveforms
(Buck Operation)



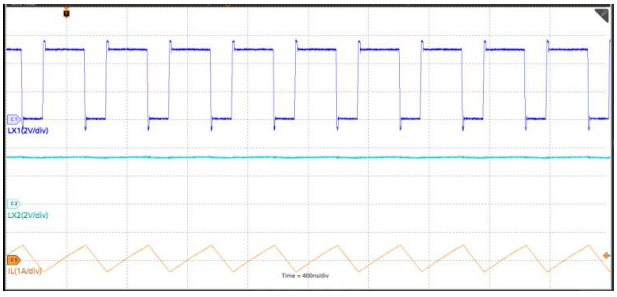
VIN=3.3V, PFM, T_A=25°C, V_O=3.3V, I_O=100mA

Figure 8 PFM Switching Waveforms
(Buck-Boost Operation)



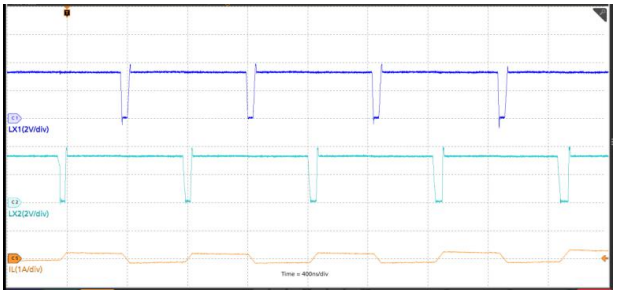
VIN=2.5V, PFM, T_A=25°C, V_O=3.3V, I_O=100mA

Figure 9 PFM Switching Waveforms
(Boost Operation)



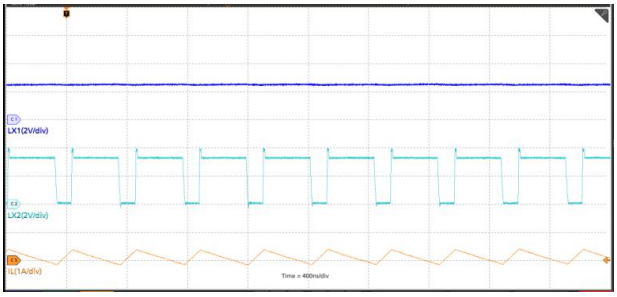
VIN=5V, FPWM, T_A=25°C, V_O=3.3V, I_O=100mA

Figure 10 PWM Switching Waveforms
(Buck Operation)



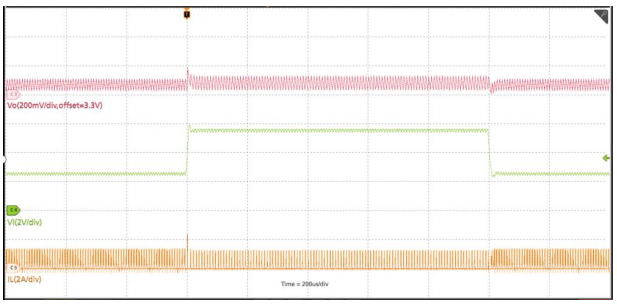
VIN=3.3V, FPWM, T_A=25°C, V_O=3.3V, I_O=100mA

Figure 11 PWM Switching Waveforms
(Buck-Boost Operation)



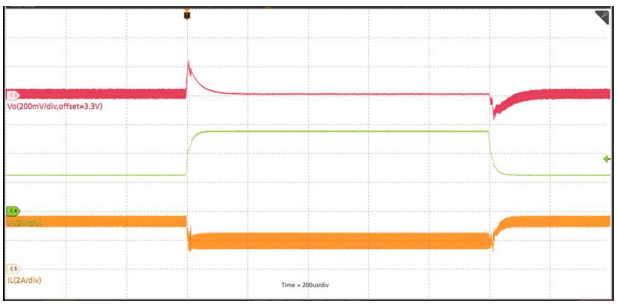
VIN=2.5V, FPWM, T_A=25°C, V_O=3.3V, I_O=100mA

Figure 12 PWM Switching Waveforms
(Boost Operation)



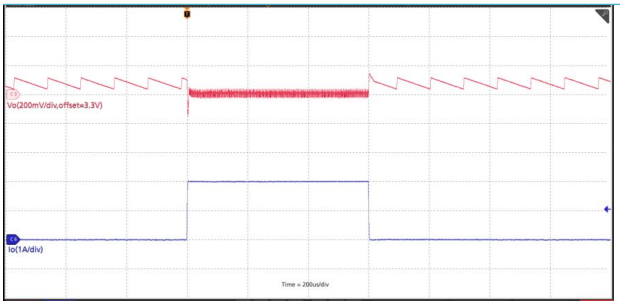
VIN=2.5V to 5.5V, PFM, T_A=25°C, V_O=3.3V, I_O=200mA

Figure 13 Line Transient Response



VIN=2.5V to 5.5V, PFM, T_A=25°C, V_O=3.3V, I_O=2A

Figure 14 Line Transient Response

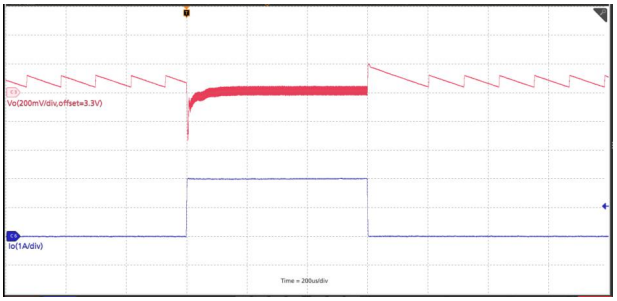


VIN=4.2V, PFM, T_A=25°C, V_O=3.3V, I_O=10mA to 2A

Figure 15 Load Transient Response (Buck)

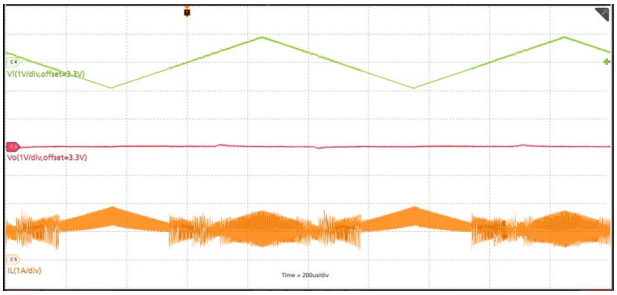
VIN=3.3V, PFM, T_A=25°C, V_O=3.3V, I_O=10mA to 2A

Figure 16 Load Transient Response (Buck-Boost)



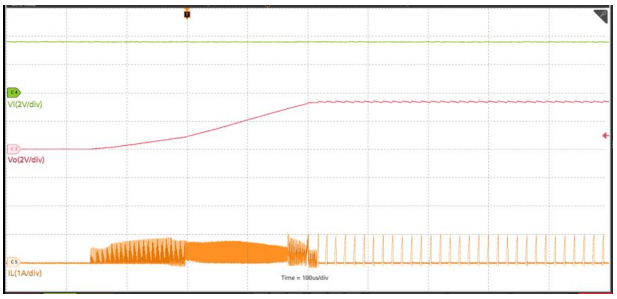
VIN=2.6V, PFM, T_A=25°C, V_O=3.3V, I_O=10mA to 2A

Figure 17 Load Transient Response (Boost)



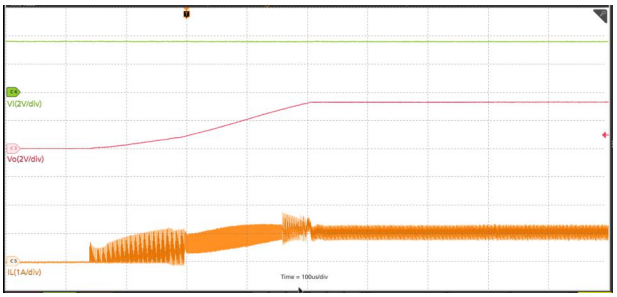
VIN=3.3V ± 0.9V, FPWM, T_A=25°C, V_O=3.3V, R_L=3.3Ω

Figure 18 Line Sweep (PWM)



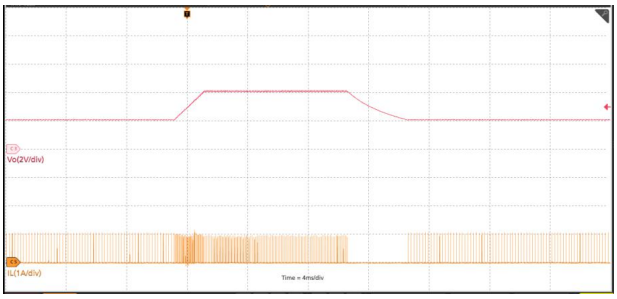
VIN=3.6V, PFM, T_A=25°C, V_O=3.3V, R_L=33Ω

Figure 19 Start-Up waveforms
(Light load)



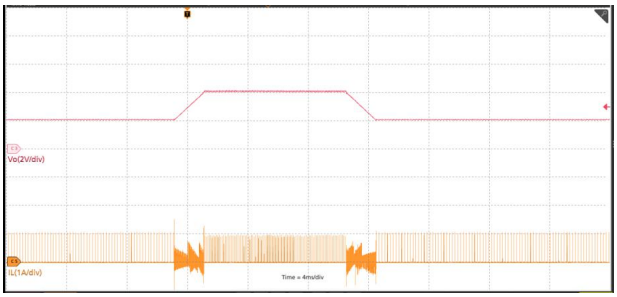
VIN=3.6V, PFM, T_A=25°C, V_O=3.3V, R_L=3.3Ω

Figure 20 Start-Up Waveforms
(Heavy Load)



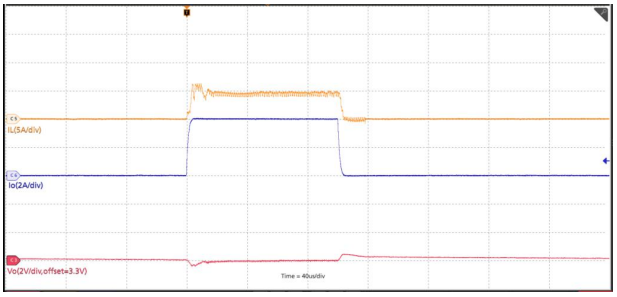
VIN=3.6V, PFM, T_A=25°C, V_O=2V to 4V, R_L=330Ω

Figure 21 Dynamic Voltage Scaling (PFM)



VIN=3.6V, PFM, T_A=25°C, V_O=2V to 4V, RPWM, R_L=330Ω

Figure 22 Dynamic Voltage Scaling (RPWM)



VIN=3.6V, PFM, TA=25°C, V_O=3.3V

Figure 23. Overcurrent Protection

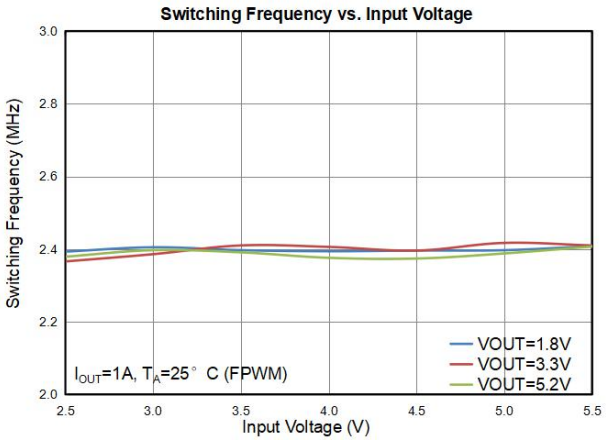


Figure 24. Switching Frequency versus Input Voltage

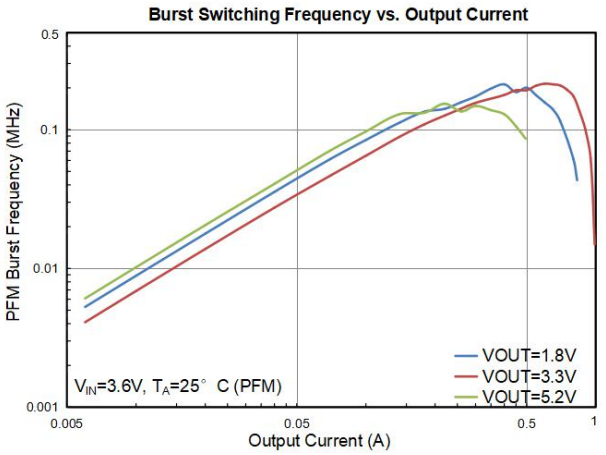


Figure 25. Burst Switching Frequency versus Output Current

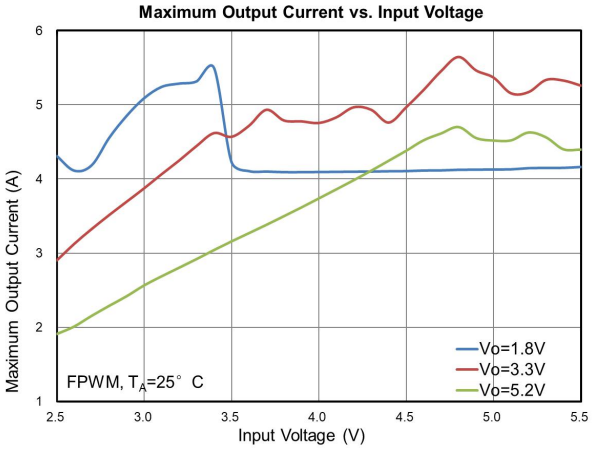


Figure 26. Maximum Output Current versus Input Voltage

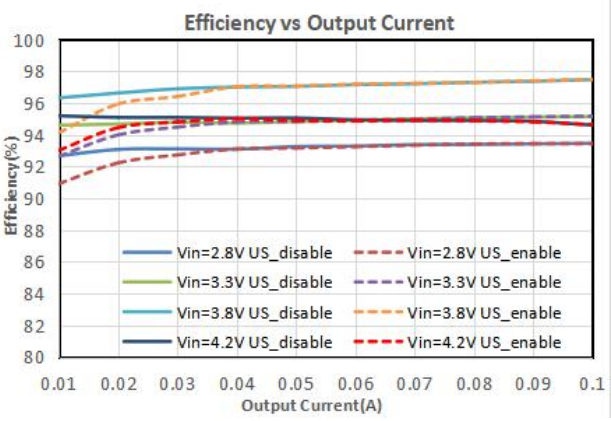


Figure 27. Efficiency versus Output Current (Ultra-sonic enable VS disable)

4 Detailed Description

4.1 Overview

The Au8310 device is synchronous buck-boost converter with two integrated P-channel MOSFETs and two integrated N- channel MOSFETs. This enables the device to keep high efficiency over the complete input voltage and output voltage range.

To regulate the output voltage at all possible input voltage condition, the device automatically switches from buck operation to boost operation and back as required by the configuration.

The device operates as a buck converter when $V_{IN} > V_{OUT}$, and as a boost converter when $V_{IN} < V_{OUT}$. When $V_{IN} \approx V_{OUT}$, the device operates in buck-boost mode. The device provides a seamless transition between buck and boost operation. There is no mode of operation in which all 4 switches are switching at the same time. The RMS current through the switches and the inductor is kept at a minimum, to minimize switching and conduction losses. Controlling the switches this way allows the converter to always keep higher efficiency.

The device provides a seamless transition between buck and boost operation.

4.2 Functional Block Diagram

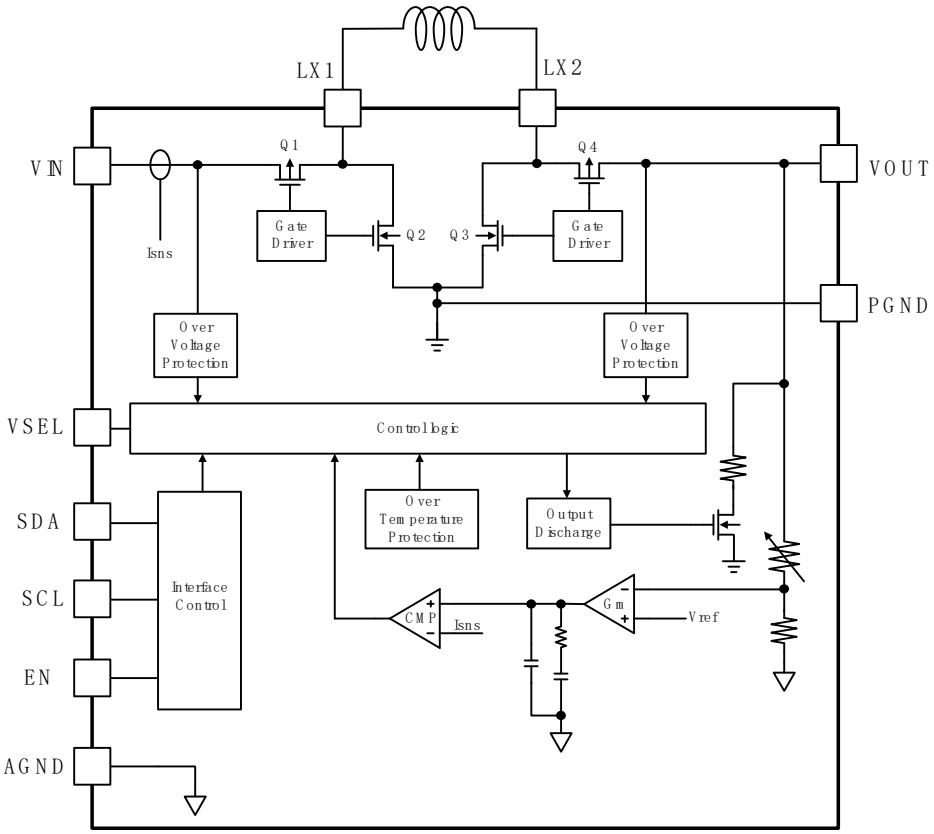


Figure 28 Block diagram

4.3 Feature Description

4.3.1 Buck-Boost Conversion Topology

The Au8310 operates in either Buck or Boost mode. When operating in conditions where V_{IN} is close to V_{OUT}, the Au8310 alternates between Buck and Boost mode as necessary to provide a regulated output voltage.

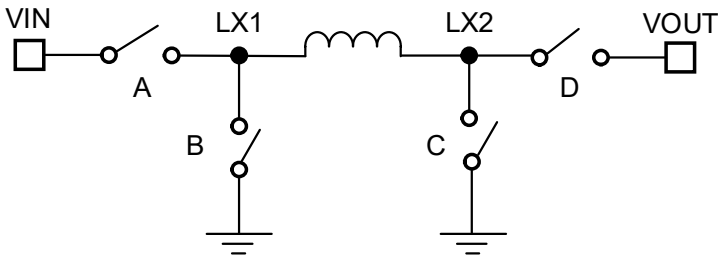


Figure 29 Buck-Boost Topology

4.3.2 PWM Operation

In Buck PWM mode, Switch D is continuously ON and Switch C is continuously OFF. Switches A and B operate as a synchronous buck converter when in this mode.

In Boost PWM mode, Switch A remains ON and Switch B remains OFF. Switches C and D operate as a synchronous boost converter when in this mode.

4.3.3 PFM Operation

During PFM operation in Buck mode, Switch D is continuously ON, and Switch C is continuously OFF. Switches A and B operate in Discontinuous mode during PFM operation. During PFM operation in Boost and Buck-Boost mode, the Au8310 closes Switch A and Switch C to ramp up the current in the inductor. When the inductor current reaches a certain threshold, the device turns off Switches C and turn on Switch D, so it works at bypass mode. After a fixed time, the chip turns on Switches B and D. With Switches B and D ON, output voltage increases as the inductor current ramps down.

In most operating conditions, there will be multiple PFM pulses to charge up the output capacitor. These pulses continue until V_{OUT} has achieved the upper threshold of the PFM hysteretic controller. Switching then stops and remains stopped until V_{OUT} decays to the lower threshold of the hysteretic PFM controller.-

4.3.4 Internal Supply and References

Referring to the “Block Diagram” in Figure 28, the Au8310 provides two power input pins. The VIN pin not only supplies input power to the DC/DC converter, but also provides an operating voltage source required for stable VREF generation. Separate ground pins (AGND and GND) are provided to avoid problems caused by ground shift due to the high switching currents.

4.3.5 Enable Input

The device uses a precise EN pin and is enabled by asserting the EN pin High. When the voltage applied on EN is over the rising threshold, it starts to work. Driving EN below falling threshold invokes a power-down mode in which most internal device functions are disabled.

You can also use the ENABLE bit in the Control register to enable and disable the output of the converter (see the Register Map).

Table 11 Device Enable Truth Table

Enable Pin (EN)	ENABLE Bit	Device State	Output State
0	X	Device in Shutdown	Output Discharge Active
1	0	Programming Interface Active	Output Discharge Active
1	1	Device Active	Output Enabled

4.3.6 Soft Discharge

When the device is disabled by driving EN pin LOW or ENABLE bit is set to 0, an internal NMOS switch between V_{OUT} and GND is activated to slowly discharge the output capacitor.

4.3.7 POR Sequence and Soft-Start

Asserting the EN pin HIGH allows the device to power up. The following events occur during the start-up sequence. The internal voltage reference powers up and stabilizes. The device then starts operating.

To minimize inrush current and output voltage overshoot during start-up, the device features a controlled soft start-up. After the device is enabled, the device starts all internal reference and control circuits within the enable delay time.

The soft start feature minimizes output voltage overshoot and input inrush currents. During soft-start, the reference voltage is ramped to provide a ramping VOUT voltage. While the output voltage is lower than approximately 25% of the target output voltage, switching frequency is reduced to a fraction of the normal switching frequency which is around 1MHz to aid in producing low duty cycles necessary to avoid input inrush current spikes. Once the output exceeds 25% of the target voltage, switching frequency is increased to its nominal value.

4.3.8 Internal Compensation

The buck-boost converter utilizes a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over its full operating range. No compensation design is required.

4.3.9 Operation with V_{IN} Close to V_{OUT}

When the output voltage is close to the input voltage, the Au8310 rapidly and smoothly switches between Boost and Buck mode as needed to maintain the regulated output voltage. This behavior provides excellent efficiency and very low output voltage ripple.

4.3.10 Output Voltage Selection (VSEL)

The device can generate output voltages from 1.8V to 5.2V with a resolution of 25 mV. To set the output voltage range, you must first program the RANGE bit in the Control register to select the output voltage range:

- When RANGE=0, you can program the output voltage from 1.800V to 4.975V.
- When RANGE=1, you can program the output voltage from 2.025V to 5.200V.

To set the output voltage, you must also first set VSEL pin by pulling this pin High or LOW to select the output voltage register:

- When VSEL PIN=HIGH, VOUT[6:0] = VOUT2[6:0]
- When VSEL PIN=LOW, VOUT[6:0] = VOUT1[6:0]

When you have selected the output voltage range, you can program the VOUT1 register and VOUT2 register to set the output voltage:

- When RANGE=0, VOUT=(VOUT[6:0]×0.025)+1.800V
- When RANGE=1, VOUT=(VOUT[6:0]×0.025)+2.025V

Note

To prevent output voltage transients, Ningbo Aura semiconductor recommends that you do not change the output voltage range while the converter is in operation. Instead, clear the ENABLE bit in the Control register to 0 to disable the DC/DC converter before you change the RANGE bit.

4.3.11 Dynamic Voltage Scaling

The device has a dynamic voltage scaling (DVS) function which lets you change the output voltage in a controlled way during operation. Figure 30 shows a simplified block diagram of the DVS function. The VSEL pin controls a multiplexer which selects either the VOUT1 register or the VOUT2 register to control the set voltage. The ramp control block detects when the target output voltage is different from the actual output voltage and ramps the output voltage to the target voltage in 25mV steps.

You can use the 2-bit SLEW parameter in the Control register to select one of four slew rates from 1 V/ms to 10 V/ms. The device starts a DVS ramp when you change the logic level on the VSEL pin or program to a new value in the active VOUT register.

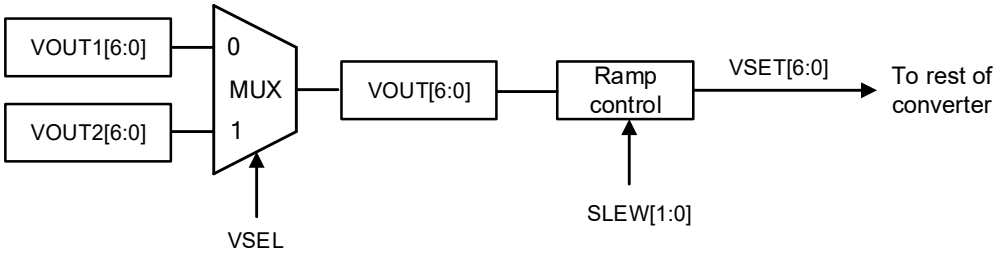


Figure 30 Dynamic Voltage Scaling Block Diagram

Note that if you change the contents of the active VOUT register or change the state of the VSEL pin during start-up (that is, before the end of the soft start), the converter uses the new value immediately and does not ramp gradually to the final value. Figure 31 shows the timing diagram when you use the VSEL pin to change between the output voltage values in the VOUT1 and VOUT2 registers.

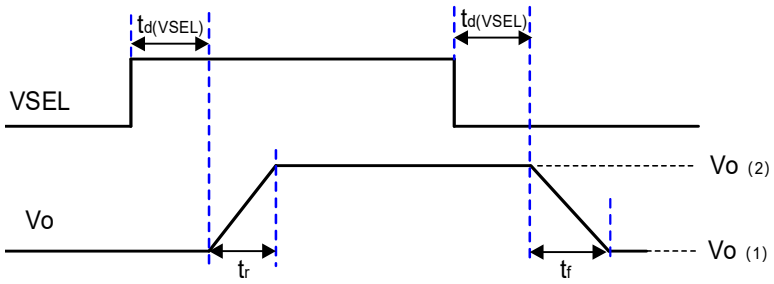


Figure 31 DVS Timing Diagram Using the VSEL Pin

$$t_r = t_f = \frac{|V_o(2) - V_o(1)|}{SR}$$

Where:

- $V_o(1)$ is the output voltage set by the VOUT1 register.
- $V_o(2)$ is the output voltage set by the VOUT2 register.
- SR is the slew rate set by the SLEW bits in the CONTROL register.

Figure 32 shows the timing diagram when you use the I2C interface to change the output voltage value in one of the VOUT registers.

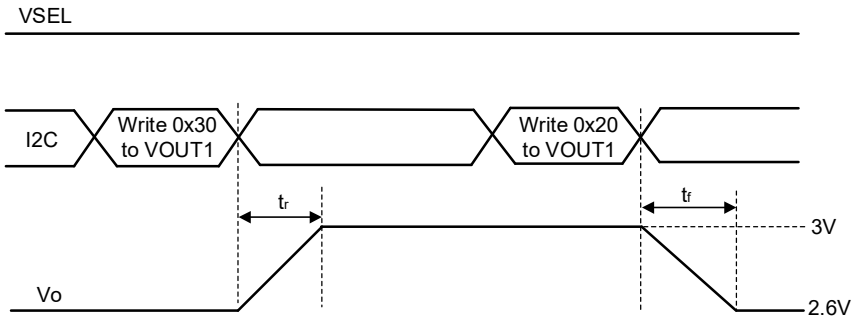


Figure 32 DVS Timing Using the I2C Interface

$$t_r = t_f = \frac{|3.0 - 2.6|}{SR}$$

Where SR is the slew rate set by the SLEW bits in the CONTROL register.

4.4 Protection Functions

4.4.1 Input Voltage Protection (IVP)

Under certain operating conditions, current can flow from the output of the device to the input. For example, this can occur during dynamic voltage scaling when the output ramps down to a lower voltage and the VOUT pin sinks current from the output capacitor. Under such conditions, if the voltage input source supplying the device cannot sink current, the voltage on the VIN pin can rise uncontrollably. Under force PWM operation (FPWM=1) and in order to make sure the input voltage stays within the permitted range, the device will enter Auto PFM mode if the voltage on the VIN pin is greater than 5.7V. The device automatically starts to switch and back to force PWM operation again when the voltage on the VIN pin is less than 5.6V.

The device sets the $\overline{PG}$ bit in the Status register when an input overvoltage event occurs. The device clears the $\overline{PG}$ bit if the Status register is read when the power-not-good condition no longer exists.

4.4.2 Over Current Protection

The device has a clamp circuit which limits the peak inductor current in the event of an overload. The exact value of the output current during an overload changes with the operating conditions (V_{IN} and V_{OUT}) and the switching mode (buck, buck-boost, or boost).

Overloads increase the power dissipation in the device, which increases its temperature. If the device becomes too hot, the thermal shutdown function turns off the converter. When the device cools down, the thermal shutdown function automatically turns on the converter again. Thus, under a permanent overload condition, the device can periodically turn on and off, as it cools down and then heats up.

4.4.3 Over Voltage Protection

The device has the over-voltage protection function to avoid the output voltage exceeding critical values. When V_{OUT} hits the output OVP rising threshold, it enters Hi-Z mode, all the switches stop switching. It recovers from OVP when V_{OUT} drops below falling threshold.

4.4.4 Thermal Shutdown

A built-in thermal protection feature protects the Au8310 if the die temperature reaches 150°C (typical). At this die temperature, the regulator is completely shut down. The die temperature continues to be monitored in this thermal shutdown mode. When the die temperature falls to 130°C (typical), the device resumes normal operation. When exiting thermal shutdown, the Au8310 executes its soft-start sequence.

When the device detects an over temperature condition, it sets the TSD bit in the Status register to 1. The device clears the TSD bit to 0 if you read the Status register when the junction temperature of the device is less than 130°C.

4.4.5 Power Good

The device has a power-good function which indicates if the output of the DC/DC converter is in regulation or not. The device detects a power-good condition when the output voltage is greater than 95% of its nominal value and detects a power-not-good condition when the output voltage is less than 90% of its nominal value.

When a power-not-good condition occurs, the device sets the $\overline{PG}$ bit in the Status register to 1. The device clears the $\overline{PG}$ bit to 0 if you read the Status register when a power-good condition exists.

4.4.6 Load Disconnect

During device shutdown, the input is disconnected from the output. This prevents any current flow from the output to the input or from the input to the output.

4.4.7 Output Discharge

The device actively discharges the output when the EN pin is low or ENABLE bit=0 or VIN pin voltage is lower than UVLO threshold.

4.5 Device Functional Modes

The device has two functional modes: OFF and ON. The device enters the ON mode when the voltage on the VIN pin is higher than the UVLO threshold and a high logic level is applied to the EN pin. The device enters the OFF mode when the voltage on the VIN pin is lower than the UVLO threshold or a low logic level is applied to the EN pin.

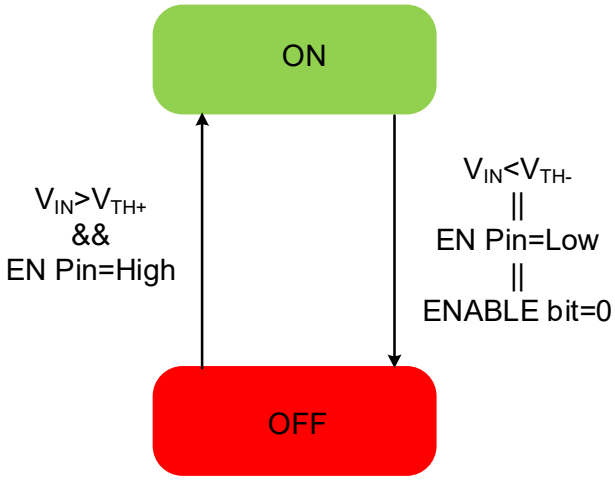


Figure 33 Device Functional Modes

4.6 I2C Serial Interface

The Au8310 supports a bidirectional bus-oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the Au8310 operates as a slave device in all applications. The SCL and SDA pin need external pull-up resistor connected with a proper voltage level. Pull the SCL and SDA pins to a proper voltage level if the I2Cinterface is not used. All communication over the I2C interface is conducted by sending the MSB of each byte of data first.

4.6.1 Set Power Save Mode with I2C Interface

Depending on the load current, in order to provide the best efficiency over the complete load range, the device works in PWM mode at load currents of approximately 250mA or higher. At lighter loads, the device switches automatically into Power Save Mode to reduce power consumption and extend battery life. The FPWM bit [3] of register 0x01 is used to select between the two different operation modes. To enable Power Save Mode, the bit must be set 0. Set this bit 1 to force PWM.

4.6.2 Set Ultrasonic Mode with I2C Interface

The switching frequency decreases when it is very light load and it enters audio frequency that causes acoustic noise. To limit the minimal switching frequency, Ultrasonic mode is required. For Au8310A4, write 1 to Ultra-Sonic bit [4] of register 0x01 to force it enable Ultrasonic function. For Au8310A5, write 1 to Ultra-Sonic bit [4] of register 0x01 to force it disable Ultrasonic function. The minimal switching frequency is 60kHz at no load.When it is very light load,the Ultrasonic mode enable efficiency is a little lower than it is disable.Figure 27 shows the efficiency difference comparison.

4.6.3 Ramp-PWM Operation (RPWM)

If Ramp-PWM operation is enabled, the device operates in forced-PWM when it ramps from one output voltage to another during dynamic voltage scaling. This function is useful if the device is needed to operate in power-save mode, but at the same time make sure that dynamic voltage scaling ramps the output voltage up and down in a controlled way. If the device operates in power-save mode and Ramp-PWM is disabled, the device cannot always control the ramp from a higher output voltage to a lower output voltage, because in power-save mode the device cannot sink current (see **Figure** 34).

To enable Ramp-PWM operation, set the RPWM bit in the Control register to 1. To disable Ramp-PWM operation, clear the RPWM bit in the Control register to 0.

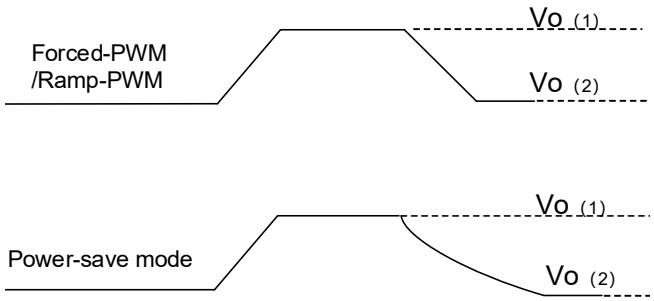


Figure 34 Ramp-PWM Operation

4.6.4 Digital Slew Rate Control

When changing voltages using the I2C interface, the Au8310 can be programmed to control the slew rate of voltage increase or decrease as it transits from one voltage setting to the next. Details about the digital slew rate settings can be found in Table .

4.7 Register Map

Au8310 has five I2C accessible registers which include CONTROL Register, STATUS Register, DEVID Register, VOUT1 Register and VOUT2 Register. The registers are volatile: they lose their contents if the voltage on the VIN pin becomes less than 1.5V(typical) or a low logic level is applied to the EN pin.

4.7.1 CONTROL Register (Address = 0x01) [Default = 0x20]

This register configures the device.

Table 12 CONTROL Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0b	Reserved
6	RANGE	R/W	0b	This bit selects the output voltage range. 0b = Low range (1.800V to 4.975V) 1b = High range (2.025V to 5.200V)
5	ENABLE	R/W	1b	This bit enables and disables the output of Au8310. 0b = Output is disabled 1b = Output is enabled
4	Ultra-Sonic	R/W	0b	A4: This bit controls ultrasonic mode. 0b=Ultrasonic mode disabled 1b=Ultrasonic mode enabled A5: This bit controls ultrasonic mode. 0b=Ultrasonic mode enabled 1b=Ultrasonic mode disabled
3	FPWM	R/W	0b	This bit controls forced-PWM operation. 0b=Forced-PWM operation disabled 1b=Forced-PWM operation enabled
2	RPWM	R/W	0b	This bit controls ramp-PWM operation.
1-0	SLEW	R/W	00b	The two bits control the slew rate of the converter when the output voltage setting is changed to a new value. 00b=1.0V/ms 01b=2.5V/ms 10b=5.0V/ms 11b=10.0V/ms

NOTE: R/W=Read/Write; R=Read only

4.7.2 STATUS Register (Address = 0x02) [Default = 0x00]

This register contains the device status. A read operation to this register clears the status bits.

Table 13 STATUS Register Field Descriptions

Bit	Field	Type	Default	Description
7-2	RESERVED	R	000000b	Reserved
1	TSD	R	0b	This bit shows the status of the thermal shutdown function. This bit is cleared if the STATUS register is read when the over temperature condition no longer exists. 0b=Temperature good 1b=An over temperature event was detected
0	$\overline{PG}$	R	0b	This bit shows the status of the output power good comparator. This bit is cleared if the STATUS register is read when the power-not- good condition no longer exists. 0b=Power good 1b=A power-not-good event was detected

NOTE: R/W=Read/Write; R=Read only

4.7.3 DEVID Register (Address = 0x03) [Default = 0xD0]

This register identifies the die revision of the device.

Table 14 DEVID Register Field Descriptions

Bit	Field	Type	Default	Description
7-4	MANUFACTURER	R	1101b	These bits identify the device manufacturer.
3-2	MAJOR	R	00b	The two bits identify the major die revision.

Bit	Field	Type	Default	Description
				00b=A (initial silicon) 01b=B (first major revision) 10b=C (second major revision) 11b=D (third major revision)
1-0	MINOR	R	00b	The two bits identify the minor die revision. 00b=0 (initial silicon) 01b=1 (first minor revision) 10b=2 (second minor revision) 11b=3 (third minor revision)

NOTE: R/W=Read/Write; R=Read only

4.7.4 VOUT1 Register (Address = 0x04) [Default = 0x3C]

This register sets the device output voltage when the VSEL pin is low.

Table 15 VOUT1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0b	Reserved
6-0	VOUT1	R/W	0111100b	These bits set the output voltage of the converter when the VSEL pin is low. The output voltage in volts is 1.8+(VOUT1[6:0] × 0.025) (RANGE bit =0b) (default =3.3V) The output voltage in volts is 2.025+(VOUT1[6:0] × 0.025) (RANGE bit =1b) (default =3.525V)

NOTE: R/W=Read/Write; R=Read only

4.7.5 VOUT2 Register (Address = 0x05) [Default = 0x42]

This register sets the device output voltage when the VSEL pin is high.

Table 16 VOUT2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	RESERVED	R	0b	Reserved
6-0	VOUT2	R/W	1000010b	These bits set the output voltage of the converter when the VSEL pin is high. The output voltage in volts is 1.8+(VOUT2[6:0] × 0.025) (RANGE bit =0b) (default =3.45V) The output voltage in volts is 2.025+(VOUT2[6:0] × 0.025) (RANGE bit =1b) (default =3.675V)

NOTE: R/W=Read/Write; R=Read only

4.8 Programming

4.8.1 Serial Interface Description

I2C is a 2-wire serial interface developed by Philips Semiconductor, now NXP Semiconductors (see UM10204: I2C-Bus Specification and User Manual, Revision 6). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I2C-compatible devices connect to the I2C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The device works as a slave and supports the following data transfer modes, as defined in the I2C-Bus Specification: Standard-mode (100 kbps), Fast-mode (400 kbps) and Fast-mode Plus (1 Mbps). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as supply voltage remains above 2.2V.

The data transfer protocol for standard and fast modes is exactly the same, therefore it is referred to as F/S- mode in this document. The device supports 7-bit addressing; 10-bit addressing and general call address are not supported. The device 7-bit address is 75h (1110101b).

To make sure that the I2C function in the device is correctly reset, it is recommended that the I2C master initiates a STOP condition on the I2C bus after the initial power up of SDA and SCL pull-up voltage.

4.8.2 Standard-, Fast-, Fast-Mode Plus Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 35. All I2C-compatible devices should recognize a start condition.

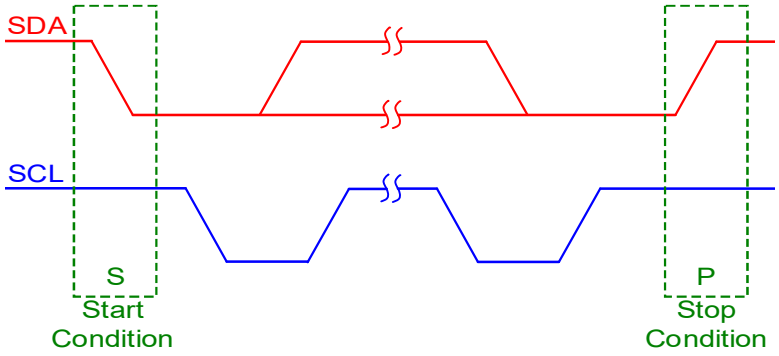


Figure 35 START and STOP Conditions

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure36). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 37) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.

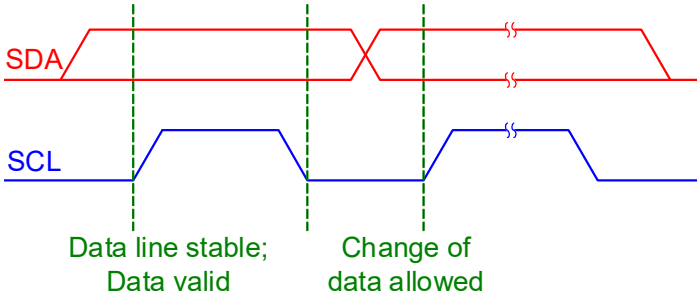


Figure 36 Bit Transfer on the Serial Interface

The master generates further SCL cycles to either transmit data to the slave (R/W bit1) or receive data from the slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary. To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high. This

releases the bus and stops the communication link with the addressed slave. All I2C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section will result in 00h being read out.

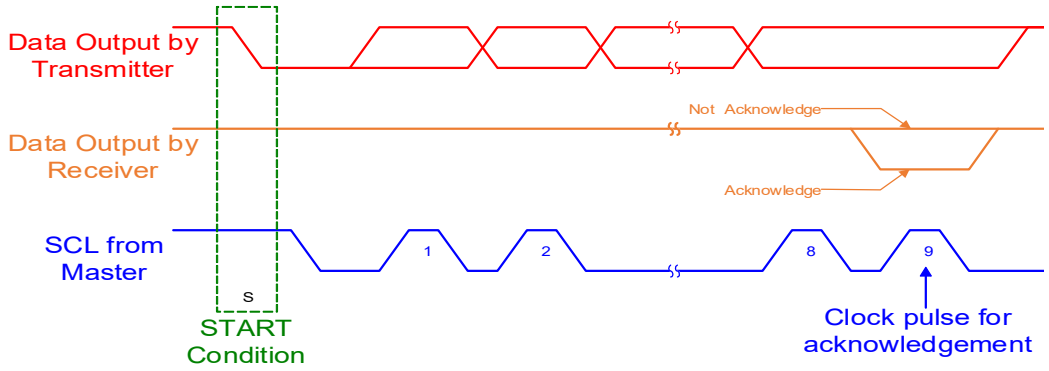


Figure 37 Acknowledge on I2C Bus

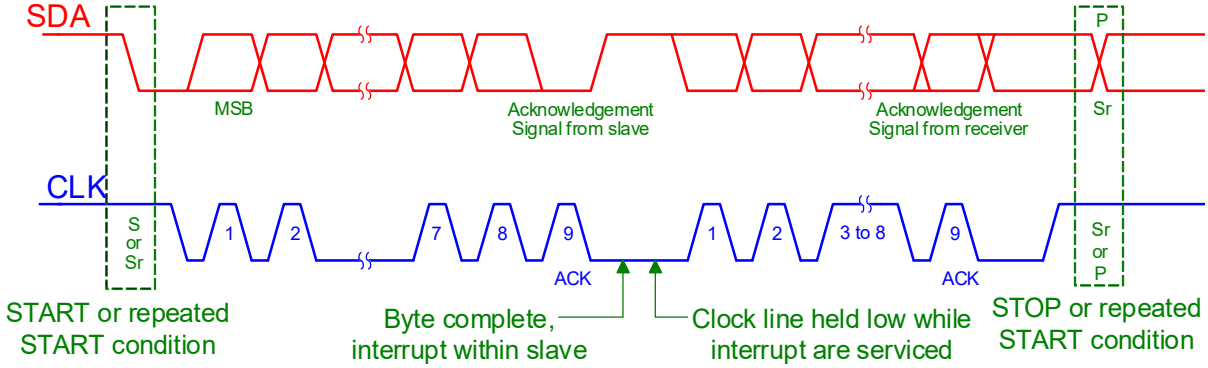


Figure 38 Bus Protocol

4.8.3 I2C Update Sequence

A single update requires a start condition, a valid I2C slave address, a register address, and a data byte. To acknowledge the receipt of each byte, the device pulls the SDA line low during the high period of a single clock pulse. The device performs an update on the falling edge of the acknowledge signal that follows the last byte.

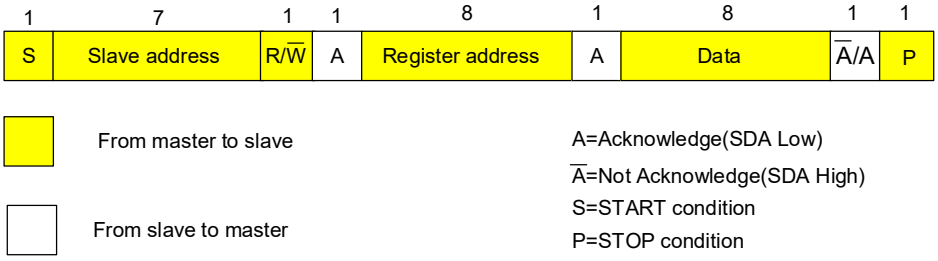


Figure 39 Write Data Transfer Format in Standard, Fast and Fast-Plus Modes

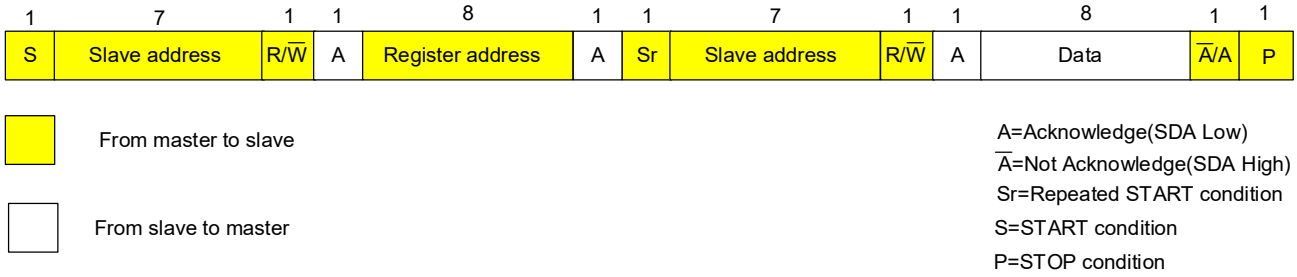


Figure 40 Read Data Transfer Format in Standard, Fast and Fast-Plus Modes

5 Application and Implementation

Note

Information in the following applications sections is not part of the Ningbo Aura Semiconductor component specification and Ningbo Aura Semiconductor does not warrant its accuracy or completeness. Ningbo Aura Semiconductor's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

5.1 Application Information

The Au8310 device is a highly integrated synchronous buck-boost DC/DC converter. This device is used to convert a wide range input voltage to a wide DC output voltage.

5.2 Typical Application

The application schematic of Figure 41 was developed to meet the requirements above. This circuit is available as the Au8310 evaluation module. The design procedure is given in this section.

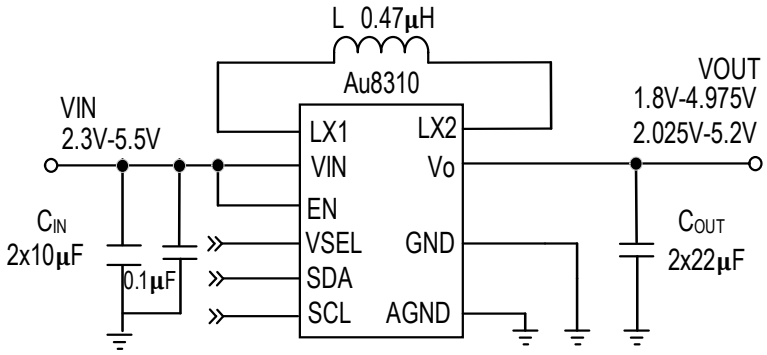


Figure 41 Typical Application Circuit

5.3 Inductor Selection

Use an inductor with high frequency core material (for example, ferrite core) to minimize core losses and provide good efficiency. The inductor must be able to handle the peak switching currents without saturating.

A 0.47 μH inductor is recommended. Select an inductor with low DCR and low core losses to provide good efficiency. In applications in which radiated noise must be minimized, a toroidal or shielded inductor can be used.

The saturation current of the inductor must be greater than the maximum inductor current in your application. To include sufficient margin for worst-case and transient operating conditions, and inductor with saturation current that is at least 20% higher than the maximum inductor current in your application is recommended. The maximum current in the inductor occurs when the device operates in boost mode and the following is true:

- The input voltage is at its minimum value.
- The output voltage is at its maximum value.
- The output current is at its maximum value.

To calculate the maximum inductor current, first use Equation1 to calculate the maximum duty cycle during boost operation (which is when the maximum inductor current occurs).

$$D = \frac{V_{OUT}-V_{IN}}{V_{OUT}} \qquad \text{Equation1}$$

Where D is the duty cycle, V_{IN} is the input voltage, V_{OUT} is the output voltage.

When V_{OUT}=5V, V_{IN}=2.5V, $D = \frac{5-2.5}{5} = 0.5$

Then use Equation2 to calculate the maximum inductor current.

$$I_{LM} = \frac{I_O}{\eta\times(1-D)} + \frac{D\times V_{IN}}{2\times f\times L} \qquad \text{Equation2}$$

Where:

- I_{LM} is the peak inductor current
- I_O is the output current
- η is the converter efficiency (assume 90%)
- f is the switching frequency(2.5MHz)
- L is the inductance(0.47μH).

So $$I_{LM} = \frac{2}{0.9\times(1-0.5)} + \frac{0.5\times2.5}{2\times2.5M\times0.47\mu} = 5A$$

Based on the above calculation, following inductors on Table17 are recommended to use.

Table 17 Inductor vendor information

Vendor	Part Number	Description	Dimension (mm)	Website
Coilcraft	XFL4015-471ME	0.47μH, ±20%, DCR_{MAX}=8.36mΩ, I_{SAT}=5.4A	4.0x4.0x1.5	www.coilcraft.com
muRata	DFE201612E-R47M	0.47μH, ±20%, DCR_{MAX}=26mΩ, I_{SAT}=5.5A	2.0x1.6x1.2	www.murata.com
Wurth	784383340047	0.47μH, ±20%, DCR_{MAX}=26.4mΩ, I_{SAT}=9A	3.0x3.0x1.2	www.we-online.com

5.4 VIN and VOUT Capacitor Selection

Steady state and transient response operation performance also depend on input voltage stability or not. At least 2x10μF input capacitors are recommended to prevent input voltage instability with application operation. Also you must place capacitors as close as possible to the VIN and GND pins of the IC. If the input supply is more than a few centimeters from the device, we recommend you add some bulk capacitance to the ceramic bypass capacitors. A 47μF electrolytic capacitor is a typical selection for the bulk capacitance. A 0.1μF is also necessary to filter high frequency noise in input.

The ripple voltage is an important index for choosing output capacitor. This portion consists of two parts. One is the product of ripple current with the ESR of the output capacitor, while the other part is formed by the charging and discharging process of the output capacitor. The recommended Vo capacitor value is 2x22μF.The output capacitance does not have an upper limit; you can make it as big as you want.

Table 18 Capacitor Vendor Information

Manufacture	Series	Website
Murata	X5R/X7R	www.murata.com
Taiyo Yuden	X5R/X7R	www.t-yuden.com
TDK	X5R/X7R	www.tdk.com
Wurth	X5R/X7R	www.we-online.com

6 Power Supply Recommendation

The device is designed to operate with a DC supply voltage in the range of 2.2V to 5.5V. If the input supply is more than a few centimeters from the device, Aura recommends adding some bulk capacitance to the ceramic bypass capacitors. A 47uF electrolytic capacitor is a typical selection for the bulk capacitance.

7 Layout

7.1 Layout Guidelines

- Layout is a critical portion of good power supply design. See Figure 41 for a PCB layout example.
- The top layer contains the main power traces for VIN, Vo, LX1 and LX2. Also on the top layer are connections for the remaining pins of the Au8310 and a large top-side area filled with ground.
- There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric.
- Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the ground connections.
- Since the LX1 and LX2 connection are the switching node, the output inductor should be located close to the LX1 and LX2 pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling.
- The output filter capacitor ground should use the same power ground trace as the VIN input bypass capacitor.
- Try to minimize this conductor length while maintaining adequate width.

7.2 Layout Example

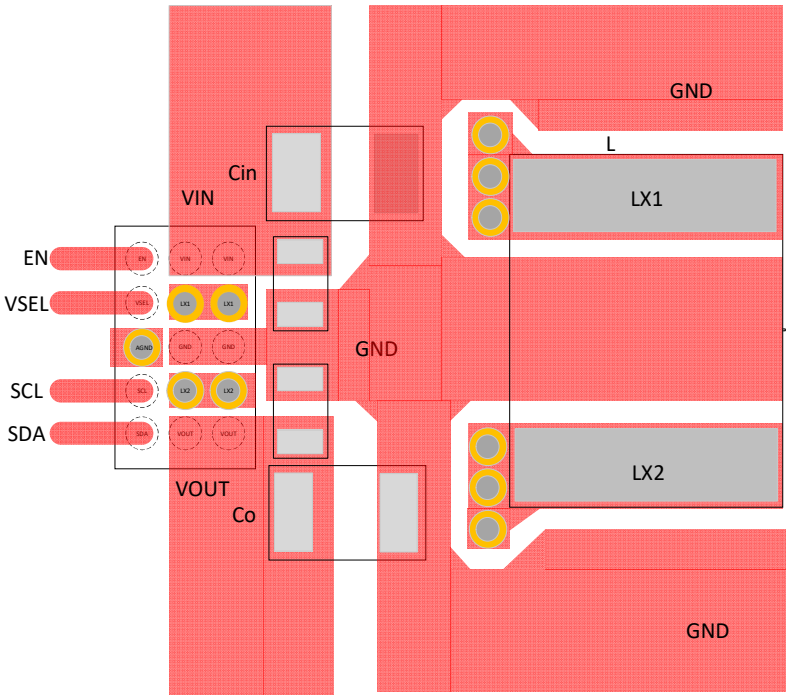


Figure 42 Layout Example

8 Device Comparison Table

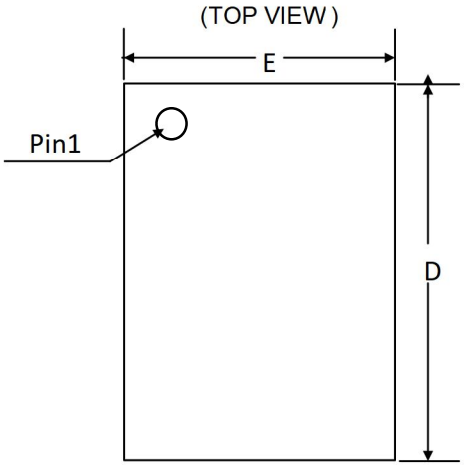
Table 19 Device Comparison Table

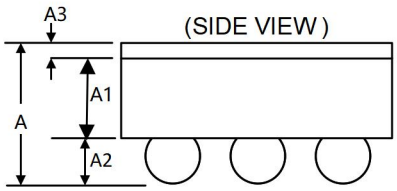
Part Number	Ultra-Sonic Mode Initial state	Ultra-Sonic Bit Default
Au8310A4	Disable	0b
Au8310A5	Enable	0b

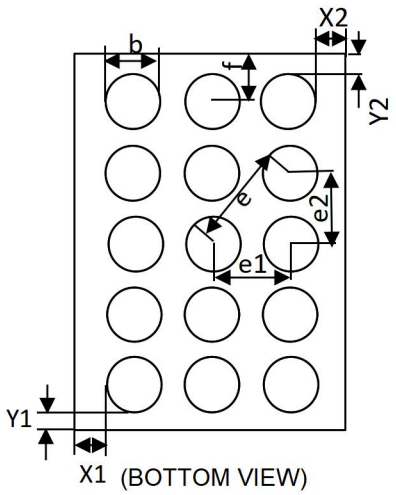
9 Package and ordering information

9.1 Package Outline Drawing

DIE SIZE BALL GRID ARRAY





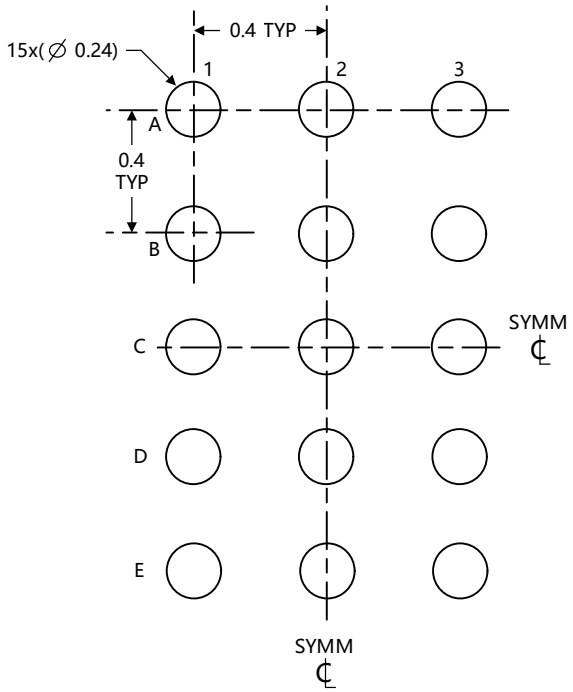


Symbol	Nominal(um)	Min(um)	Max(um)
A	580	535	625
A1	355	330	380
A2	200	180	220
A3	25BSC		
E	1380	1350	1410
D	2280	2250	2310
e	565.685 REF		
e1	400		
e2	400		
f	340		
b	260	230	290
X1	160 REF		
Y1	210 REF		
X2	160 REF		
Y2	210 REF		

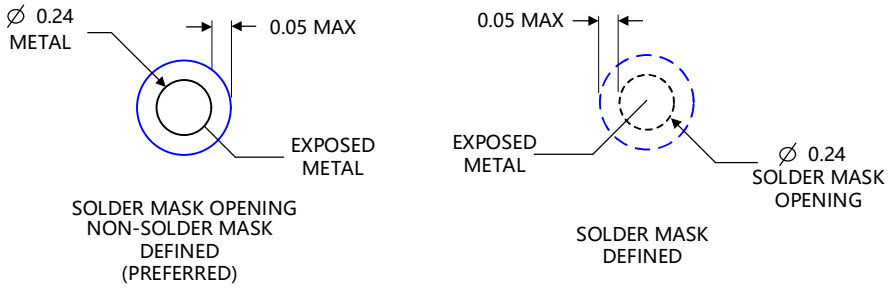
NOTES:

(1) All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only.
(2) This drawing is subject to change without notice.

DIE SIZE BALL GRID ARRAY



LAND PATTERNEXAMPLE
EXPOSED METAL SHOWN
SCALE:X40

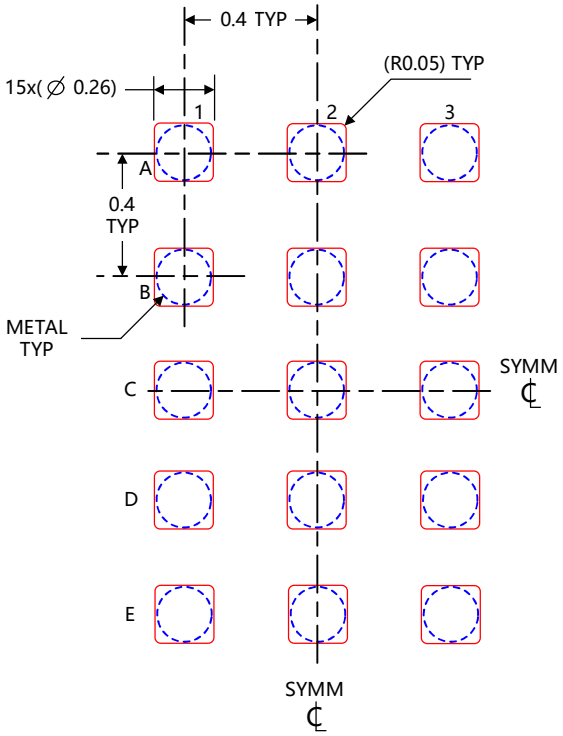


SOLDER MASK DETAILS
NOT TO SCALE

NOTES: (continued)

(3) Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1mm THICK STENCIL
SCALE:40X

NOTES: (continued)

(4) Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

9.2 Ordering Information

Table 20 Ordering Information

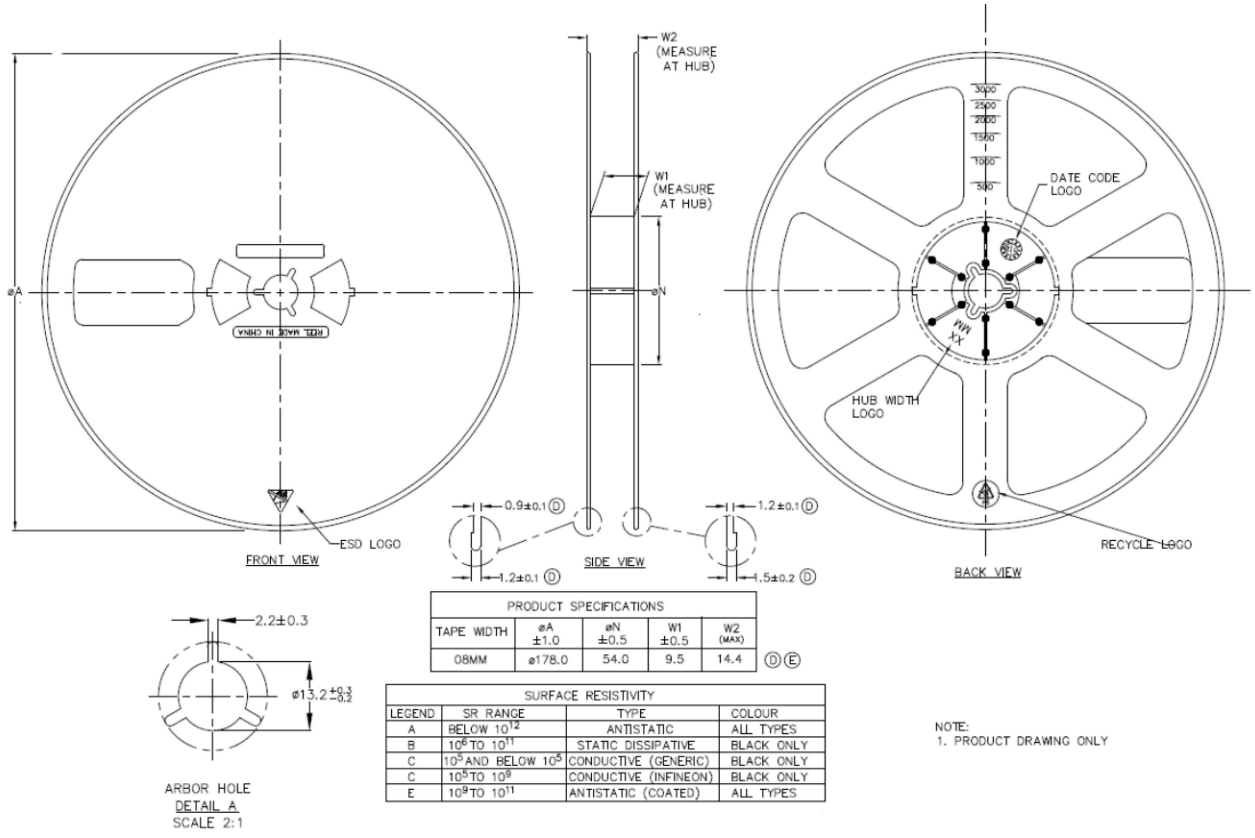
Ordering Part Number (OPN) (Note1,2)	Part Marking (Note3)	Tape and Reel (Units)	Temp Range (°C)	Package (RoHS Compliant)	PKG. DWG. #
Au8310A4-WMR	Au8310A4	3k	-40 to +85	15 Ball WLCSP	15-WLCSP 1.38x2.28 mm POD
Au8310A5-WMR	Au8310A5	3k	-40 to +85	15 Ball WLCSP	15-WLCSP 1.38x2.28 mm POD

Note:

(1) Add an R at the end of the OPN to denote tape and reel packing information.
(2) RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
(3) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

9.3 Package Materials Information

9.3.1 Tape and Reel Information

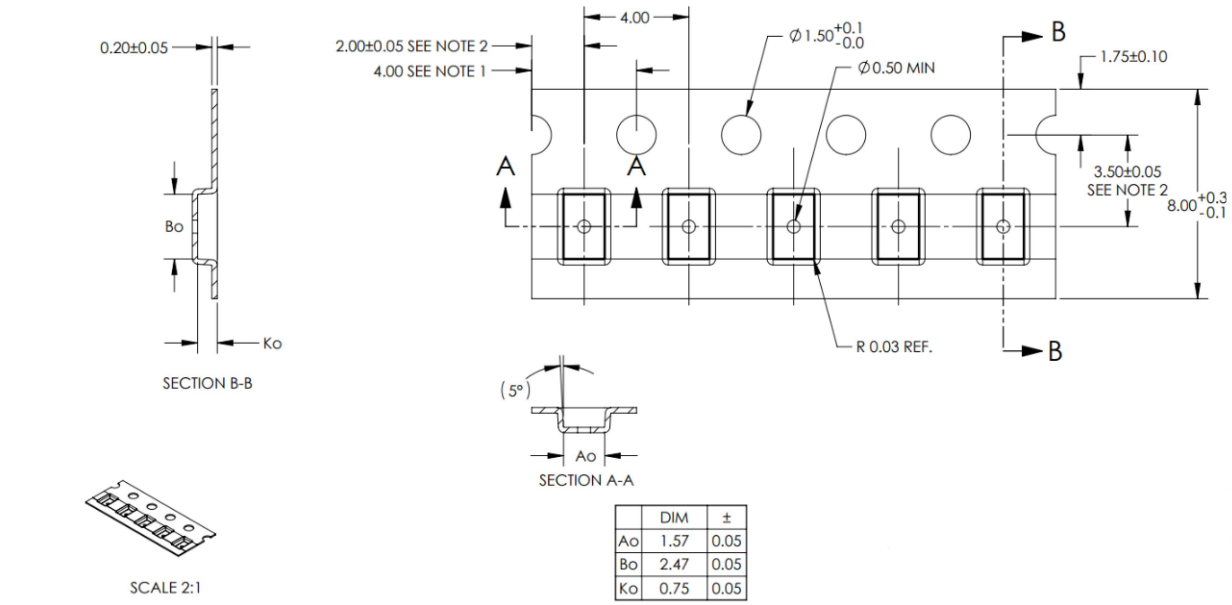


PRODUCT SPECIFICATIONS

TAPE WIDTH	øA ±1.0	øN ±0.5	W1 ±0.5	W2 (MAX)
08MM	ø178.0	54.0	9.5	14.4

SURFACE RESISTIVITY

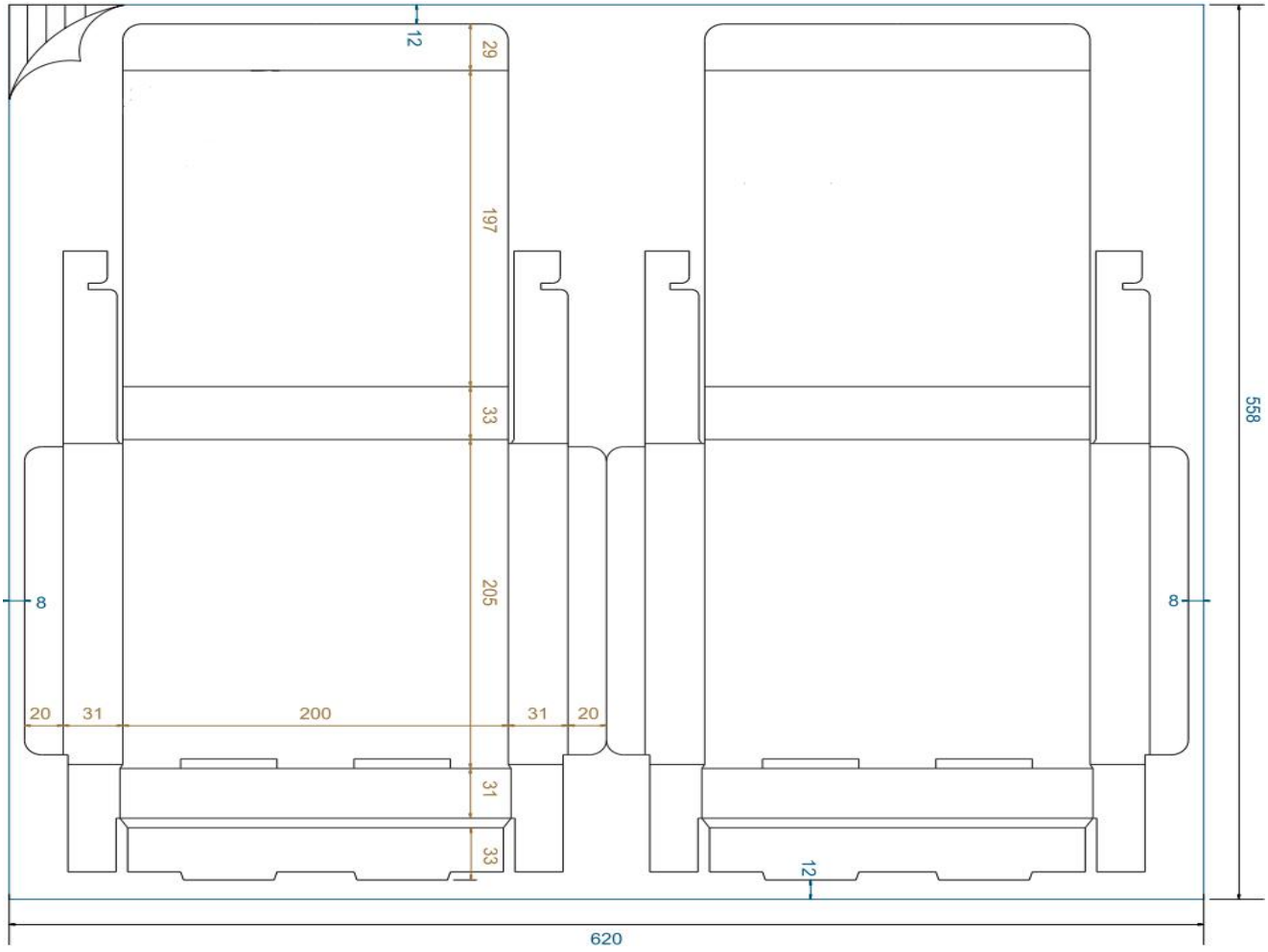
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} AND BELOW 10^{5}	CONDUCTIVE (GENERIC)	BLACK ONLY
C	10^{5} TO 10^{9}	CONDUCTIVE (INFINEON)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC (COATED)	ALL TYPES



	DIM	±
Ao	1.57	0.05
Bo	2.47	0.05
Ko	0.75	0.05

NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE.
3. Ao AND Bo ARE MEASURED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

9.3.2 Tape and Reel box information



10 Revision History

Table 20 Revision History

Version Number	Date	Description	Author
0.1	2nd, July 2019	Advanced Datasheet created	
0.2	20th, Aug 2019	Add layout guide and key feature description	
0.3	30th, Oct 2019	Add I2C function description	
0.4	8th, Nov 2019	Updated the EC table	
0.5	25th, Dec 2019	Add ultrasonic mode, add by pass mode into register, update efficiency curve	
0.6	05th, Jan 2020	Add ultrasonic mode, remove by pass mode, update efficiency curve	
0.7	14th, Mar 2020	Add DVS function description and control diagram, soft-start/ PG function	
v0p1_FR 1.0	18th, Apr 2020	Add more figures	
v0p2_FR 1.0	29th, May 2020	Add more figures and optimize the Reflink	
0.8	18th, Aug 2020	Change some parameters, OVP, OCP function modification, inductor selection, some graph modification	
0.9	10th, March 2021	POD change	
v0p1_FR 1.0	7th, May 2021	Add ordering information	
Preliminary	30th, June 2021	Update test data	
Released	4th, Aug 2021	Released datasheet	
Released	25th, Jan 2022	Add OPN(Au8310A5-WMR)	

11 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.